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Preliminary Amendment

IN THE CLAIMS

Please cancel claims 28, 32-33, 69-70, and 77 without prejudice.

Please amend claims 29-31 as follows below.

The following is a listing of claims replacing all prior versions, and listings, of claims in the application:

Listing of Marked Up Claims:

- 1 1. (Original) A system comprising:
 - 2 a radio frequency integrated circuit including
 - 3 a single bit modulator to convert an analog
 - 4 signal into a serial digital bit stream, and
 - 5 an output driver coupled to the single bit
 - 6 sigma delta modulator, the output driver to drive
 - 7 the serial digital bit stream out from the radio
 - 8 frequency integrated circuit;
 - 9 and
 - 10 a digital signal processing integrated circuit
 - 11 including
 - 12 an input receiver coupled to the output
 - 13 driver of the radio frequency integrated circuit,
 - 14 the input receiver to receive the serial digital
 - 15 bit stream, and
 - 16 a decimator coupled to the input receiver,
 - 17 the decimator to receive the serial digital bit
 - 18 stream, lower a sampling rate of the serial
 - 19 digital bit stream and convert the serial digital
 - 20 bit stream into parallel digital data samples.

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1 2. (Original) The system of claim 1, wherein
2 the digital signal processing integrated circuit
3 further includes
4 a demodulator to digitally demodulate the
5 parallel digital data samples into data words for
6 further signal processing by the digital signal
7 processing integrated circuit.

1 3. (Original) The system of claim 1, wherein
2 the single bit modulator is a single bit sigma
3 delta modulator.

1 4. (Original) The system of claim 1, wherein
2 the single bit modulator is a single bit delta
3 modulator.

1 5. (Original) The system of claim 1, wherein
2 the single bit modulator is a single bit analog to
3 digital converter and a modulator coupled together.

1 6. (Original) The system of claim 1, wherein
2 the output driver has a low voltage output swing,
3 the output driver to drive the serial digital bit
4 stream out of the radio frequency integrated circuit
5 with the low voltage output swing.

1 7. (Original) The system of claim 6, wherein
2 the input receiver to receive the serial digital
3 bit stream with the low voltage output swing.

1 8. (Original) The system of claim 7, wherein

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2 the input receiver further to increase the low
3 voltage output swing of the serial digital bit stream
4 within the digital signal processing integrated circuit.

1 9. (Original) The system of claim 6, wherein
2 the low voltage output swing between a high logic
3 level and a low logic level is less than an output
4 swing between a high logic level and a low logic level
5 of a three volt complementary metal oxide semiconductor
6 (CMOS) process technology.

1 10. (Original) The system of claim 6, wherein
2 the low voltage output swing between a high logic
3 level and a low logic level is less than an output
4 swing between a high logic level of 1.8 volts and a low
5 logic level of 0.2 volts.

1 11. (Original) The system of claim 8, wherein
2 the output driver translates first voltage levels
3 of a first output voltage swing of the serial digital
4 bit stream into second voltage levels with a second
5 output voltage swing less than the first output voltage
6 swing, and
7 the input receiver translates the second voltage
8 levels of the second output voltage swing into third
9 voltage levels with a third output voltage swing
10 greater than the second output voltage swing.

1 12. (Original) The system of claim 11, wherein
2 the third voltage levels are substantially the
3 same as the first voltage levels.

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1 13. (Original) The system of claim 1, wherein
2 the output driver is double ended and generates a
3 differential signal to represent the serial digital bit
4 stream, and
5 the input receiver has a differential input to
6 receive the differential signal to represent the serial
7 digital bit stream.

1 14. (Original) The system of claim 13, wherein
2 the output driver is a low voltage differential
3 signaling transmitter to generate a low voltage
4 differential output signal with a low voltage
5 differential swing, and
6 the input receiver is a low voltage differential
7 signaling receiver to receive the low voltage
8 differential output signal with the low voltage
9 differential swing.

1 15. (Original) The system of claim 14, wherein
2 the low voltage differential swing is at least 100
3 milli-volts.

1 16. (Original) The system of claim 1, wherein
2 the serial digital bit stream is a rectangular
3 waveform.

1 17. (Original) The system of claim 1, wherein
2 the radio frequency integrated circuit is a
3 receiver.

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1 18. (Original) The system of claim 1, wherein
2 the radio frequency integrated circuit is a
3 transceiver.

1 19. (Original) The system of claim 1, wherein
2 a delta sigma clock is coupled to the single bit
3 sigma delta modulator, a frequency of the delta sigma
4 clock to provide a data rate in the serial digital bit
5 stream.

1 20. (Original) The system of claim 19, wherein
2 the frequency of the delta sigma clock is
3 programmable to provide various data rates in the
4 serial digital bit stream for various wireless
5 communication systems.

1 21. (Original) The system of claim 1, wherein
2 a low frequency reference clock couples between
3 the radio frequency integrated circuit and the digital
4 signal processing integrated circuit to synchronize
5 clock signals of each.

1 22. (Original) The system of claim 21, wherein
2 the low frequency reference clock synchronizes a
3 sigma delta clock of the radio frequency integrated
4 circuit with a local clock of the digital signal
5 processing integrated circuit.

1 23. (Original) A radio frequency integrated circuit
2 comprising:

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3 at least one gain amplifier to couple to an
4 antenna to receive a first wireless radio frequency
5 signal of a first selectable carrier frequency;
6 at least one down converter coupled to the at
7 least one gain amplifier, the at least one down
8 converter to extract a first analog signal from the
9 first wireless radio frequency signal;
10 at least one single bit sigma delta modulator
11 coupled to the at least one down converter, the at
12 least one single bit sigma delta modulator to convert
13 the first analog signal into a first serial digital bit
14 stream; and
15 at least one output driver coupled to the at least
16 one single bit sigma delta modulator, the at least one
17 output driver to provide a low voltage output swing of
18 the first serial digital bit stream to reduce noise
19 generation as the first serial digital bit stream is
20 coupled to another integrated circuit.

1 24. (Original) The radio frequency integrated circuit of
2 claim 23, further comprising
3 a second gain amplifier to couple to the antenna
4 to simultaneously receive a third wireless radio
5 frequency signal of a third selectable carrier
6 frequency;
7 a second down converter coupled to the second gain
8 amplifier, the second down converter to extract a third
9 analog signal from the third wireless radio frequency
10 signal;
11 a second single bit sigma delta modulator coupled
12 to the second down converter, the second single bit

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13 sigma delta modulator to convert the third analog
14 signal into a third serial digital bit stream; and
15 a second output driver coupled to the second
16 single bit sigma delta modulator, the second output
17 driver to provide a low voltage output swing of the
18 third serial digital bit stream to reduce noise
19 generation as the third serial digital bit stream is
20 coupled to another integrated circuit.

1 25. (Original) The radio frequency integrated circuit of
2 claim 23, wherein
3 the at least one gain amplifier is a variable gain
4 amplifier or a switched gain amplifier.

1 26. (Original) The radio frequency integrated circuit of
2 claim 24, wherein
3 the at least one gain amplifier and the second
4 gain amplifier are variable gain amplifiers or switched
5 gain amplifiers.

1 27. (Original) The radio frequency integrated circuit of
2 claim 23, wherein
3 the radio frequency integrated circuit is a radio
4 frequency receiver integrated circuit.

1 28. (Cancelled)

1 29. (Currently Amended) The radio frequency integrated
2 circuit of claim [[28]] 23, wherein
3 the first selected carrier frequency ~~and the~~
4 ~~second selected carrier frequency~~ are is selected from

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5 a set of carrier frequencies of a first selected
6 wireless communication system.

1 30. (Currently Amended) The radio frequency integrated
2 circuit of claim 29, wherein

3 the first selected wireless communication system
4 is selected from the set of Universal Mobile
5 Telecommunication System (UMTS), Global System for
6 Multiple Communication (GSM), GSM Mobile Application
7 Part (GSM-MAP), General Packet Radio Protocol System or
8 General Packet Radio Service (GPRS), Enhanced Data GSM
9 Environment (EDGE), (GAT), Orthogonal Frequency-
10 Division Multiplexing (OFDM), Code Orthogonal Frequency
11 Division Multiplexing (COFDM), Block Coding,
12 Convolutional Coding, Turbo Coding, Trellis Coding,
13 Gaussian Minimum Shift Keying (GMSK), Quadrature Phase
14 Shift Keying (QPSK), Quadrature Amplitude Modulation
15 (QAM), Frequency Modulation (FM), Frequency Division
16 Multiple Access (FDMA), Time Division Multiple Access
17 (TDMA), Code Division Multiple Access (CDMA),
18 Narrowband CDMA (N-CDMA), Wideband CDMA (W-CDMA),
19 CDMA2000, CDMA2000-1XEV, CDMA2000-EVDO, CDMA2000-EDV,
20 Time Division-Synchronized Code Division Multiple
21 Access (TD-SCDMA), Third-Generation Partnership Project
22 (3GPP TDD), International Mobile Telecommunication
23 (IMT), IMT2000MC, IMT2000DS, IMT2000SC, IMT2000TC,
24 Personal Communication System (PCS), Digital
25 Communication System (DCS), Personal Digital Cellular
26 (PDC), Digital Enhanced Cordless Telecommunications
27 (DECT), Advanced Mobile Phone System (AMPS), Wireless

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28 Local Area Network (LAN) (IEEE 802.11a, IEEE 802.11b,
29 IEEE 802.11g), and Global Positioning System (GPS).

1 31. (Currently Amended) The radio frequency integrated
2 circuit of claim 29, wherein
3 the first selected carrier frequency is selected
4 from a set of carrier frequencies of a Universal Mobile
5 Telecommunication System (UMTS), Global System for
6 Multiple Communication (GSM), GSM Mobile Application
7 Part (GSM-MAP), General Packet Radio Protocol System or
8 General Packet Radio Service (GPRS), Enhanced Data GSM
9 Environment (EDGE), (GAT), Orthogonal Frequency-
10 Division Multiplexing (OFDM), Code Orthogonal Frequency
11 Division Multiplexing (COFDM), Gaussian Minimum Shift
12 Keying (GMSK), Quadrature Phase Shift Keying (QPSK),
13 Quadrature Amplitude Modulation (QAM), Frequency
14 Modulation (FM), Frequency Division Multiple Access
15 (FDMA), Time Division Multiple Access (TDMA), Code
16 Division Multiple Access (CDMA), Narrowband CDMA (N-
17 CDMA), Wideband CDMA (W-CDMA), CDMA2000, CDMA2000-1XEV,
18 CDMA2000-EVDO, CDMA2000-EDV, Time Division-Synchronized
19 Code Division Multiple Access (TD-SCDMA), Third-
20 Generation Partnership Project (3GPP TDD),
21 International Mobile Telecommunication (IMT), IMT2000MC,
22 IMT2000DS, IMT2000SC, IMT2000TC, Personal Communication
23 System (PCS), Digital Communication System (DCS),
24 Personal Digital Cellular (PDC), Digital Enhanced
25 Cordless Telecommunications (DECT), Advanced Mobile
26 Phone System (AMPS), Wireless Local Area Network (LAN)
27 (IEEE 802.11a, IEEE 802.11b, IEEE 802.11g), and Global
28 Positioning System (GPS),—and

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29 ~~the second selected carrier frequency is selected~~
30 ~~from a set of carrier frequencies of Universal Mobile~~
31 ~~Telecommunication System (UMTS), Global System for~~
32 ~~Multiple Communication (GSM), GSM Mobile Application~~
33 ~~Part (GSM-MAP), General Packet Radio Protocol System or~~
34 ~~General Packet Radio Service (GPRS), Enhanced Data GSM~~
35 ~~Environment (EDGE), (GAT), Orthogonal Frequency~~
36 ~~Division Multiplexing (OFDM), Code Orthogonal Frequency~~
37 ~~Division Multiplexing (COFDM), Gaussian Minimum Shift~~
38 ~~Keying (GMSK), Quadrature Phase Shift Keying (QPSK),~~
39 ~~Quadrature Amplitude Modulation (QAM), Frequency~~
40 ~~Modulation (FM), Frequency Division Multiple Access~~
41 ~~(FDMA), Time Division Multiple Access (TDMA), Code~~
42 ~~Division Multiple Access (CDMA), Narrowband CDMA (N-~~
43 ~~CDMA), Wideband CDMA (W-CDMA), CDMA2000, CDMA2000-1XEV,~~
44 ~~CDMA2000-EVDO, CDMA2000-EDV, Time Division Synchronized~~
45 ~~Code Division Multiple Access (TD-SCDMA), Third~~
46 ~~Generation Partnership Project (3GPP-TDD),~~
47 ~~International Mobile Telecommunication (IMT), IMT2000MC,~~
48 ~~IMT2000DS, IMT2000SC, IMT2000TC, Personal Communication~~
49 ~~System (PCS), Digital Communication System (DCS),~~
50 ~~Personal Digital Cellular (PDC), Digital Enhanced~~
51 ~~Cordless Telecommunications (DECT), Advanced Mobile~~
52 ~~Phone System (AMPS), and Wireless Local Area Network~~
53 ~~(LAN) (IEEE 802.11a, IEEE 802.11b, IEEE 802.11g).~~

1 32-33. (Cancelled)

1 34. (Original) A method for a wireless radio, the
2 method comprising:
3 receiving a first wireless radio signal;

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4 extracting a first analog signal from the first
5 wireless radio signal;
6 converting the first analog signal into a first
7 serial digital data signal;
8 providing a low voltage output swing in the first
9 serial digital data signal; and
10 transmitting the first serial digital data signal
11 with the low voltage output swing from a radio
12 frequency (RF) integrated circuit to a digital signal
13 processing (DSP) integrated circuit.

1 35. (Original) The method of claim 34, further comprising:
2 receiving a second wireless radio signal;
3 extracting a second analog signal from the second
4 wireless radio signal;
5 converting the second analog signal into a second
6 serial digital data signal;
7 providing a low voltage output swing in the second
8 serial digital data signal; and
9 transmitting the second serial digital data signal
10 with the reduced output voltage swing from the radio
11 frequency integrated circuit to the digital signal
12 processing (DSP) integrated circuit.

1 36. (Original) The method of claim 35, wherein
2 the first wireless radio signal and the second
3 wireless radio signal are simultaneously received.

1 37. (Original) The method of claim 35, wherein
2 the first analog signal and the second analog
3 signal are simultaneously extracted.

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1 38. (Original) The method of claim 35, wherein
2 the first wireless radio signal is received during
3 the time period that the second wireless radio signal
4 is received.

1 39. (Original) The method of claim 35, wherein
2 the first analog signal is extracted during the
3 time period that the second analog signal is extracted.

1 40. (Original) The method of claim 35, further comprising:
2 receiving a third wireless radio signal;
3 extracting a third analog signal from the third
4 wireless radio signal;
5 converting the third analog signal into a third
6 serial digital data signal;
7 providing a low voltage output swing in the third
8 serial digital data signal; and
9 transmitting the third serial digital data signal
10 with the low output voltage swing from a radio
11 integrated circuit to a digital signal processing (DSP)
12 integrated circuit.

1 41. (Original) The method of claim 40, wherein
2 the first wireless radio signal, the second
3 wireless radio signal, and the third wireless radio
4 signal are simultaneously received.

1 42. (Original) The method of claim 41, wherein

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2 the first analog signal, the second analog signal,
3 and the third analog signal are simultaneously
4 extracted.

1 43. (Original) The method of claim 34, further comprising:
2 receiving the first serial digital data signal
3 with the reduced output voltage swing;
4 increasing the output voltage swing in the first
5 serial digital data signal;
6 reducing a sampling frequency of the first serial
7 digital data signal; and
8 converting the first serial digital data signal
9 into a parallel digital data signal for processing by
10 the DSP integrated circuit.

1 44. (Original) The method of claim 34, wherein
2 the converting of the first analog signal into the
3 first serial digital data signal is a delta-sigma
4 modulation of the first analog signal into the first
5 serial digital data signal.

1 45. (Original) The method of claim 43, further comprising:
2 recovering data words from the parallel digital
3 data signal by digital demodulation for a predetermined
4 wireless communication system.

1 46. (Original) The method of claim 34, wherein
2 the transmitting of the first serial digital data
3 signal is over a single wire.

1 47. (Original) The method of claim 34, wherein

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2 the first serial digital data signal is a
3 differential data signal, and
4 the transmitting of the first serial digital data
5 signal is over a pair of wires.

1 48. (Original) The method of claim 34, wherein
2 the first serial digital data signal is a complex
3 differential data signal and the transmitting of the
4 first serial digital data signal is over two pairs of
5 wires,
6 a first differential data signal of the first
7 serial digital data signal is transmitted over the
8 first pair of wires, and
9 a second differential data signal of the
10 first serial digital data signal is transmitted
11 over the second pair of wires.

1 49. (Original) The method of claim 48, wherein
2 the first differential data signal is a real
3 component of a complex data signal, and
4 the second differential data signal is an
5 imaginary component of the complex data signal.

1 50. (Original) The method of claim 48, wherein
2 the first differential data signal is an in-phase
3 signal, and
4 the second differential data signal is a
5 quadrature signal with respect to the in-phase signal.

1 51. (Original) The method of claim 34, wherein

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2 the first serial digital data signal is a
3 multiphase differential data signal and the
4 transmitting of the first serial digital data signal is
5 over two pairs of wires,
6 a magnitude data signal of the first serial
7 digital data signal is transmitted over the first
8 pair of wires, and
9 a phase data signal of the first serial
10 digital data signal is transmitted over the second
11 pair of wires.

1 52. (Original) The method of claim 34, further comprising:
2 receiving a fourth serial digital data signal from
3 the DSP integrated circuit for transmission over a
4 wireless communication system;
5 converting the fourth serial digital data signal
6 from the DSP integrated circuit into a fourth analog
7 signal;
8 up-converting the fourth analog signal to a
9 selectable carrier frequency; and
10 transmitting the fourth analog signal through the
11 antenna as a fourth wireless radio frequency signal.

1 53. (Original) The method of claim 52, wherein
2 the fourth serial digital data signal from the DSP
3 integrated circuit is a low voltage output swing signal,
4 and the method further includes
5 increasing the low voltage output swing in the
6 fourth serial digital data signal from the DSP
7 integrated circuit.

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1 54. (Original) A data signal flow between a radio frequency
2 integrated circuit and a digital signal processing (DSP)
3 integrated circuit, the data signal flow comprising:
4 a first serial digital data signal flowing from
5 the radio frequency integrated circuit to the DSP
6 integrated circuit, the first serial digital data
7 signal representing a first received data signal from a
8 first wireless communication system; and
9 a second serial digital data signal flowing from
10 the radio frequency integrated circuit to the DSP
11 integrated circuit, the second serial digital data
12 signal representing a second received data signal from
13 a second wireless communication system.

1 55. (Original) The data signal flow of claim 54, wherein
2 the first serial digital data signal is a complex
3 differential data signal flowing over two pairs of
4 wires,
5 an in-phase differential data signal of the
6 first serial digital data signal flows over a
7 first pair of wires, and
8 a quadrature differential data signal with
9 respect to the in-phase differential data signal
10 of the first serial digital data signal flows over
11 a second pair of wires.

1 56. (Original) The data signal flow of claim 54, wherein
2 the first serial digital data signal is a
3 multiphase differential data signal flowing over two
4 pairs of wires,

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5 a magnitude data signal of the first serial
6 digital data signal flows over a first pair of
7 wires, and
8 a phase data signal of the first serial
9 digital data signal flows over a second pair of
10 wires.

1 57. (Original) The data signal flow of claim 54, further
2 comprising:

3 a third serial digital data signal flowing from
4 the DSP integrated circuit to the radio frequency
5 integrated circuit, the third serial digital data
6 signal representing a first transmit data signal for
7 communication over the first wireless communication
8 system.

1 58. (Original) The data signal flow of claim 57, wherein
2 the third serial digital data signal is a complex
3 differential data signal flowing over two pairs of
4 wires,

5 an in-phase differential data signal of the
6 third serial digital data signal flows over a
7 first pair of wires, and

8 a quadrature differential data signal with
9 respect to the in-phase differential data signal
10 of the third serial digital data signal flows over
11 a second pair of wires.

1 59. (Original) The data signal flow of claim 57, wherein

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2 the third serial digital data signal is a
3 multiphase differential data signal flowing over two
4 pairs of wires,
5 a magnitude data signal of the third serial
6 digital data signal flows over a first pair of
7 wires, and
8 a phase data signal of the third serial
9 digital data signal flows over a second pair of
10 wires.

1 60. (Original) The data signal flow of claim 54, wherein
2 the first serial digital data signal is a low
3 voltage differential data signal flowing over at least
4 one pair of wires.

1 61. (Original) The data signal flow of claim 57, wherein
2 the third serial digital data signal is a low
3 voltage differential data signal flowing over at least
4 one pair of wires.

1 62. (Original) The data signal flow of claim 54, wherein
2 a data rate of the first serial digital data
3 signal is variable to adapt to a selected wireless
4 communication system.

1 63. (Original) The data signal flow of claim 57, wherein
2 a data rate of the first serial digital data
3 signal, a data rate of the second serial digital data
4 signal, and a data rate of the third serial digital
5 data signal are variable to adapt to selected wireless
6 communication systems.

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1 64. (Original) The data signal flow of claim 54, wherein
2 the first serial digital data signal and the
3 second serial digital data signal simultaneously flow
4 from the radio frequency integrated circuit to the DSP
5 integrated circuit to simultaneously receive data over
6 two wireless channels of communication.

1 65. (Original) The data signal flow of claim 57, wherein
2 the first serial digital data signal, the second
3 serial digital data signal, and the third serial
4 digital data signal simultaneously flow between the
5 radio frequency integrated circuit and the DSP
6 integrated circuit to
7 simultaneously receive data over two wireless
8 channels of communication and
9 simultaneously transmit data over one
10 wireless channel of communication.

1 66. (Original) A radio frequency integrated circuit
2 comprising:
3 a plurality of gain amplifiers to couple to an
4 antenna to simultaneously receive wireless radio
5 frequency signals of selectable carrier frequencies;
6 a plurality of down converters coupled to the
7 plurality of gain amplifiers, the plurality of down
8 converters to simultaneously extract analog signals
9 from the wireless radio frequency signals; and
10 a plurality of sigma delta modulators coupled to
11 the plurality of down converters, the plurality of
12 single bit sigma delta modulators to simultaneously

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13 convert the analog signals into serial digital bit
14 streams; and
15 a plurality of output drivers coupled to the
16 plurality of single bit sigma delta modulators, the
17 plurality of output drivers to couple the serial
18 digital bit streams to another integrated circuit.

1 67. (Original) The radio frequency integrated circuit of
2 claim 66, wherein,
3 the plurality of output drivers further to reduce
4 an output voltage swing of the serial digital bit
5 streams to further reduce noise generation as the
6 serial digital bit streams are coupled to the another
7 integrated circuit.

1 68. (Original) The radio frequency integrated circuit of
2 claim 66, wherein
3 the plurality of gain amplifiers are a variable
4 gain amplifier or a switched gain amplifier.

1 69-70. (Cancelled)

1 71. (Original) A system comprising:
2 a radio frequency integrated circuit including
3 a single bit sigma delta modulator with an
4 analog input and a serial digital output, and
5 an output driver having an input coupled to
6 the serial digital output of the single bit sigma
7 delta modulator, the output driver having a
8 differential output;
9 and

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10 a digital signal processing integrated circuit
11 including
12 an input receiver coupled to the output
13 driver of the radio frequency integrated circuit,
14 the input receiver having a differential input to
15 couple to the differential output of the output
16 driver, the input receiver having a serial digital
17 output.

1 72. (Original) The system of claim 71, wherein
2 the output driver to drive a serial digital bit
3 stream out from the radio frequency integrated circuit
4 with a low voltage differential output swing to lower
5 noise.

1 73. (Original) The system of claim 72, wherein
2 the input receiver to receive the serial digital
3 bit stream with the low voltage differential output
4 swing.

1 74. (Original) The system of claim 71, wherein
2 the digital signal processing integrated circuit
3 further includes
4 a decimator coupled to the serial digital
5 output of the input receiver, the decimator having
6 a parallel digital output, and
7 a demodulator coupled to the parallel digital
8 output of the decimator.

1 75. (Original) A radio frequency integrated circuit
2 comprising:

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3 a gain amplifier having an input to couple to an
4 antenna, the gain amplifier having an analog output;
5 a down converter having an analog input coupled to
6 the analog output of the gain amplifier, the down
7 converter having an analog output;
8 a single bit sigma delta modulator having an
9 analog input coupled to the analog output of the down
10 converter, the single bit sigma delta modulator having
11 a serial digital output; and
12 an output driver having an input coupled to the
13 serial digital output of the single bit sigma delta
14 modulator, the output driver having a differential
15 output.

1 76. (Original) The radio frequency integrated circuit of
2 claim 75, wherein
3 the radio frequency integrated circuit is a radio
4 frequency receiver integrated circuit.

1 77. (Cancelled)

1 78. (Original) A system comprising:
2 a radio frequency integrated circuit including
3 a modulating analog to digital converter with
4 a single bit output, the modulating analog to
5 digital converter to convert an analog input
6 signal into a serial digital bit output stream,
7 and
8 an output driver coupled to the single bit
9 analog to digital converter, the output driver to

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10 drive the serial digital bit stream out from the
11 radio frequency integrated circuit;
12 and
13 a processor coupled to the radio frequency
14 integrated circuit.

1 79. (Original) The system of claim 78, wherein
2 the processor includes
3 an input receiver coupled to the output
4 driver of the radio frequency integrated circuit,
5 the input receiver to receive the serial digital
6 bit stream.

1 80. (Original) The system of claim 79, wherein
2 the processor is a digital signal processor and
3 further includes
4 a decimator coupled to the input receiver,
5 the decimator to receive the serial digital bit
6 stream, lower a sampling rate of the serial
7 digital bit stream, and convert the serial digital
8 bit stream into parallel digital data samples, and
9 a demodulator to digitally demodulate the
10 parallel digital data samples into data words for
11 further signal processing by the digital signal
12 processing integrated circuit.

1 81. (Original) The system of claim 79, wherein
2 the processor includes programmable instructions
3 to provide
4 a decimator coupled to the input receiver,
5 the decimator to receive the serial digital bit

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6 stream, lower a sampling rate of the serial
7 digital bit stream, and convert the serial digital
8 bit stream into parallel digital data samples; and
9 a demodulator coupled to the decimator, the
10 demodulator to digitally demodulate the parallel
11 digital data samples into data words for further
12 signal processing by the digital signal processing
13 integrated circuit.

1 82. (Original) A system comprising:
2 a radio frequency integrated circuit including
3 a modulating analog to digital converter with
4 an analog input and a serial digital output, and
5 an output driver having an input coupled to
6 the serial digital output of the modulating analog
7 to digital converter, the output driver having a
8 digital output;
9 and
10 a processor coupled to the radio frequency
11 integrated circuit.

1 83. (Original) The system of claim 82, wherein
2 the processor includes
3 an input receiver coupled to the digital
4 output of the output driver of the radio frequency
5 integrated circuit, the input receiver having a
6 digital input to couple to the digital output of
7 the output driver, the input receiver having a
8 serial digital output.

1 84. (Original) The system of claim 83, wherein

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2 the processor is a digital signal processor and
3 further includes
4 a decimator coupled to the serial digital
5 output of the input receiver, the decimator having
6 a digital output, and
7 a demodulator coupled to the digital output
8 of the decimator.

1 85. (Original) The system of claim 83, wherein
2 the processor includes programmable instructions
3 to provide
4 a decimator coupled to the serial digital
5 output of the input receiver, the decimator having
6 a digital output, and
7 a demodulator coupled to the digital output
8 of the decimator.